Introduction to the CSC Electronics

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The ATLAS Cathode Strip Chambers (CSCs) have 4 gas gaps, with anode wires running radially and precision cathode strips in the r-ϕ direction. Cathode strip pitch is 5 mm. Two "wheels" of 32 chambers each are located in the ATLAS endcap region (Figure 1).

In response to the ionization produced by a charged particle track the CSCs generate charge on a cluster of 3-5 strips. A charge deposit of about 80 fC ($5 \cdot 10^5$ electrons) per strip (most-probable Landau) is expected at the designed chamber gain and shaping time. In any given layer there may be a drift time of up to 30 ns.

The CSC electronics must be able to record the charge on the strips in a cluster accurately enough to allow interpolation to 1/100 of the strip pitch. In addition, it must buffer the analog data for the L1 trigger latency, and reject tracks which are not in time with the triggered beam crossing. The off-detector electronics may optionally be configured to identify and reject single-layer hits and tracks which do not project back to the I.P.

A block diagram of the CSC electronics chain is shown in Figure 2. Signals from the chamber are first processed by detector-mounted circuitry ("on-detector electronics"), then sent over fiber optic links to crate-mounted off-detector electronics. The on-detector electronics consists of ASM-I and ASM-II boards mounted inside Faraday shields with integral cooling plates along the narrow edge of each CSC, as shown in Figure 3 and Figure 4.

ASM-I boards interface directly to the CSC and contain custom CMOS preamplifier/shaper ASICs for charge amplification. Each ASM-I services 96 strips, 48 from each of two non-adjacent planes. Signals from two ASM-I's are routed through a transition board to the ASM-II which contains a modified version of the ATLAS Liquid Argon calorimeter sampling readout. The ASM-II performs analog buffering, digitization, and serialization of the data from the strips in response to a trigger. The ASM-II thus handles signals from 192 channels. It uses 16 twelve-channel SCA's (DMILL rad-tolerant CMOS process), 16 twelve-bit ADCs, a digital multiplexer, and two gigbit serializer/transmitters. The combined assembly of two ASM-I's, transition board, and ASM-II is labeled "ASM-PACK". All control signals for an ASM-PACK are generated by the off-detector electronics and transmitted by fiber optic link. There is one control link (toward detector) and two data links (toward counting room) per ASM-PACK.

Four ASM-II boards process the signals from all the precision strips in the CSC. In addition, there are 48 y-strips per layer which provide coarse transverse coordinate readout.These strips are served by a fifth ASM-PACK. All together, the system summary is

SYSTEM
- 2 endcaps
- 64 chambers
- 61,440 channels
- 640 ASM-PACKs
- 32 Sparsifier/RODs

CHAMBER
- 4 layers
- 960 channels (768 precision, 192 transverse)
- 5 ASM-PACKs
- 15 optical links (10 data, 5 control)

ASM-PACK
- 192 channels

- 1 ASM-II board
- 2 ASM-I boards
- 3 fiber optic links

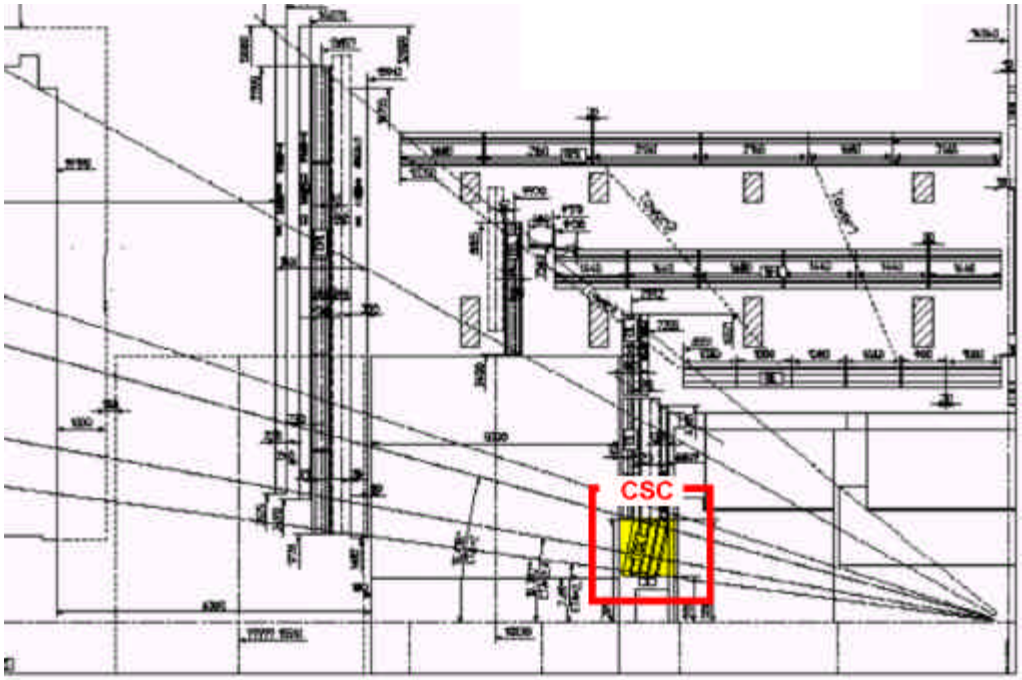
ASM-II

- 192 channels
- 2 ASM-I's
- 16 SCA ASICs
- 16 ADCs
- 2 serializer/transmitters
- 1 receiver/deserializer

ASM-I

96 channels
16 Preamp/Shaper ASICs

Figure 1 CSC Location in ATLAS; CSC endcap



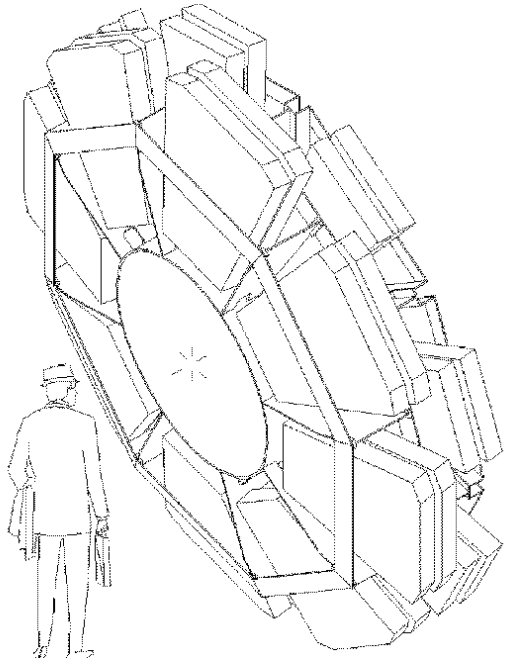


Figure 2 Signal Flow in the CSC Electronics Chain

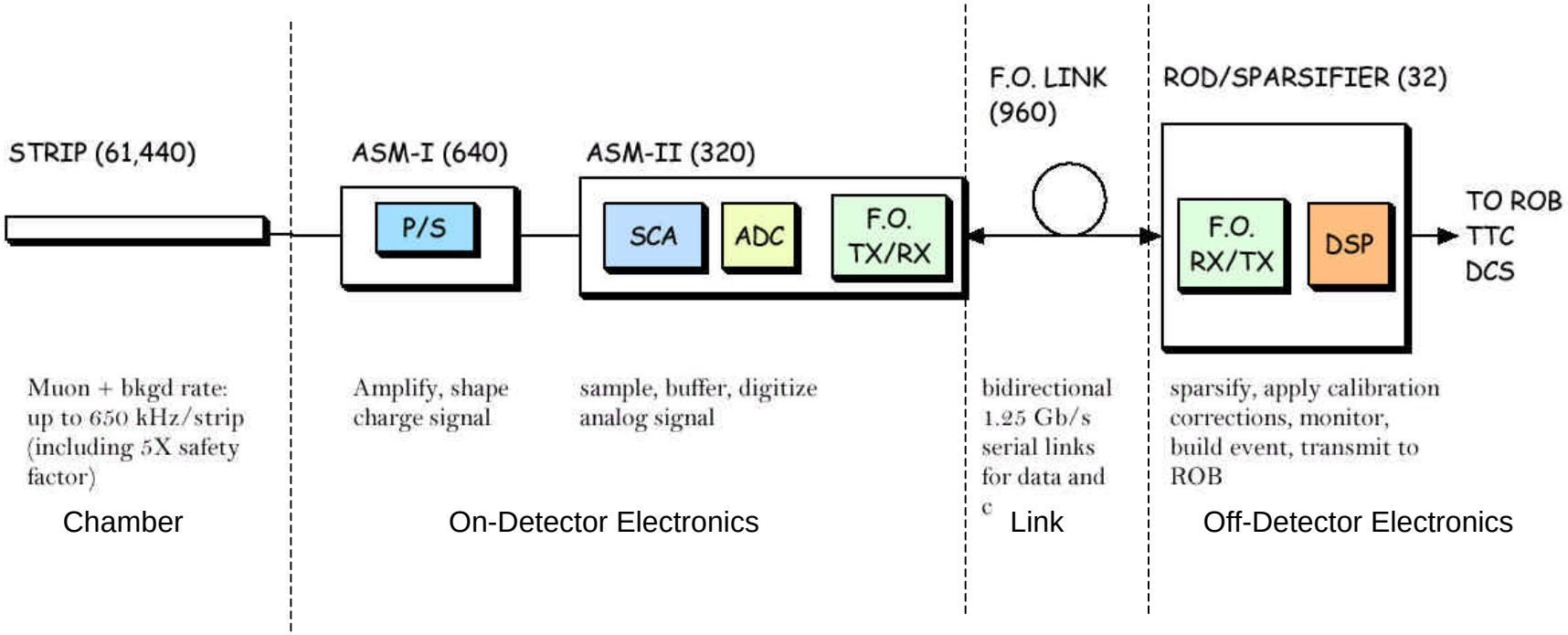
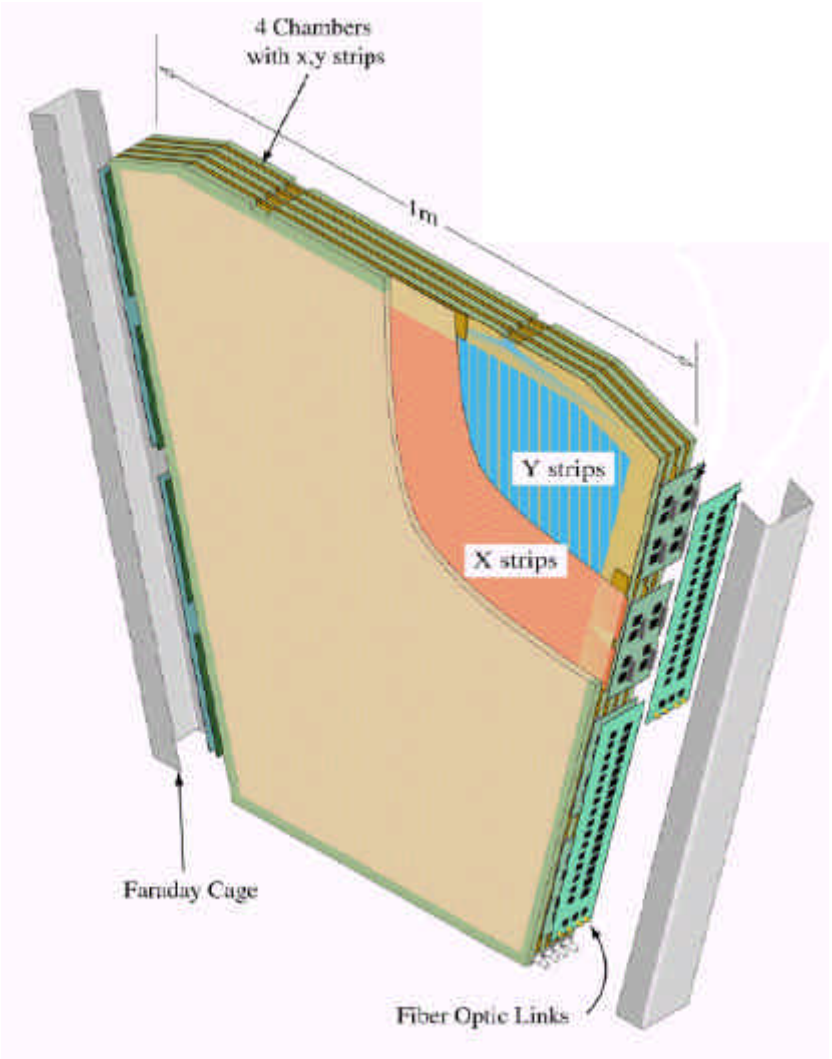


Figure 3 CSC Electronics Location on Chambers



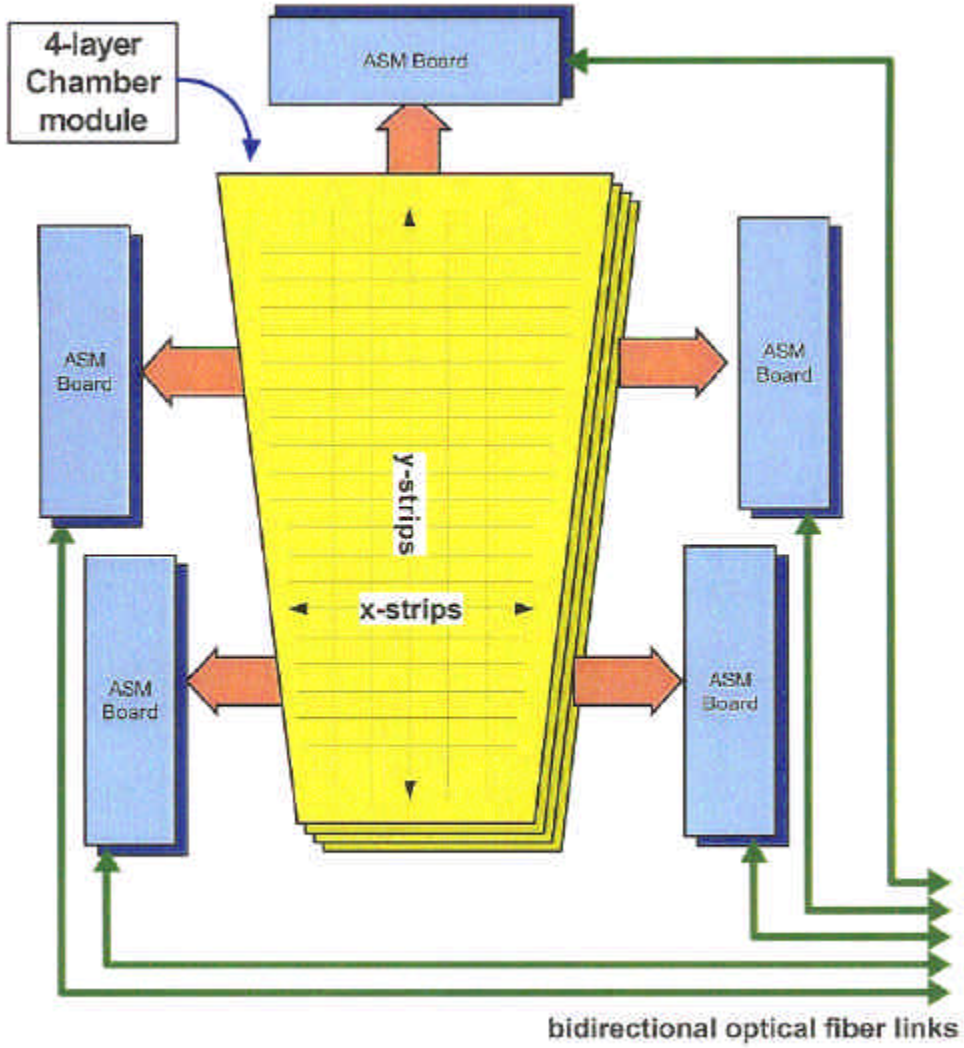
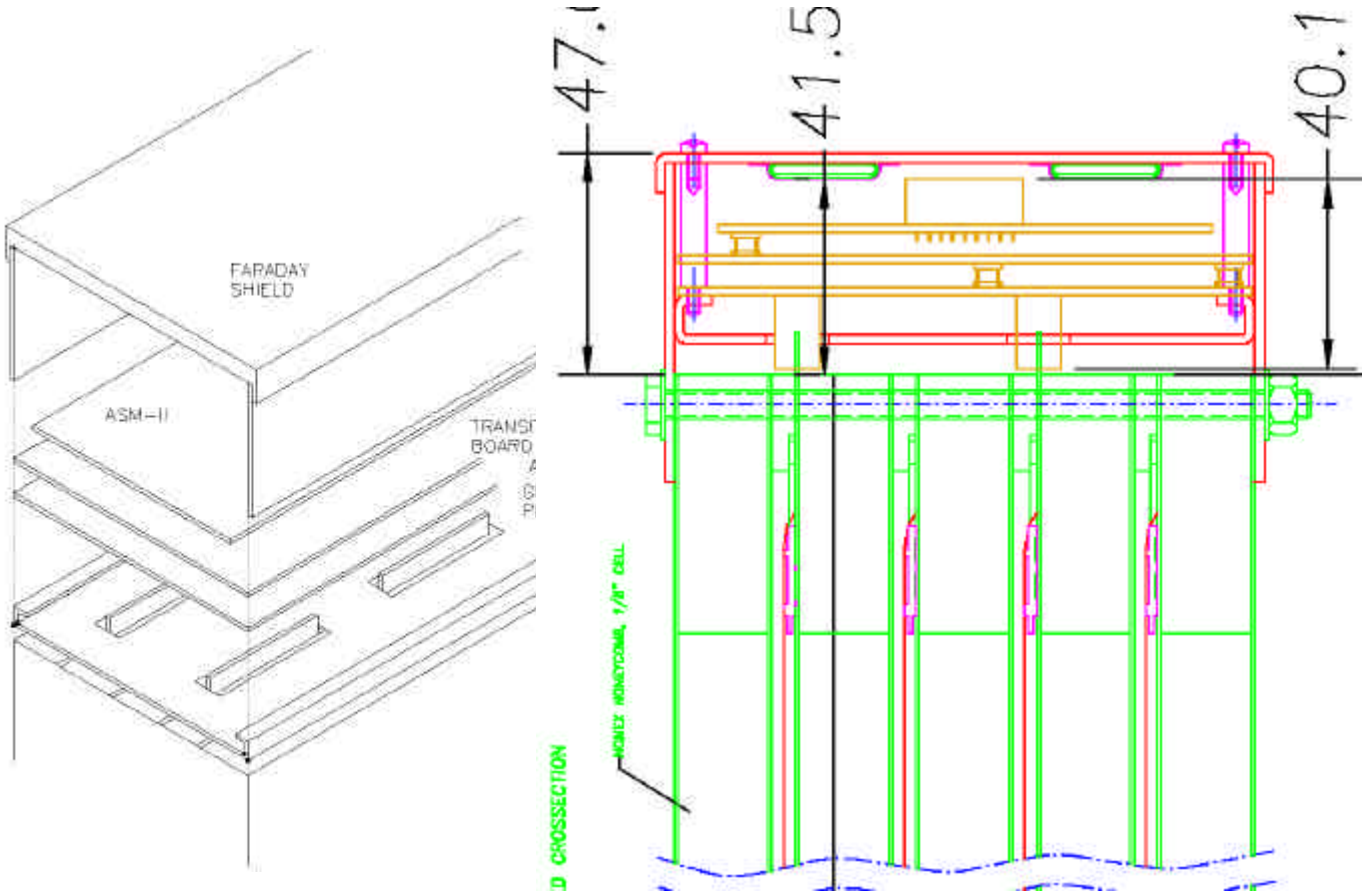


Figure 4 On-Detector Electronics Mounting



Adapting the Liquid Argon Calorimeter SCA for use with CSC

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1-Aug-00

The Switched Capacitor Analog memory (SCA) used in the ATLAS LAr readout can also be used in the muon CSC system. The requirements of the two readout systems are different and this note describes how we plan to use the Nevis/Saclay SCA in the CSC.

Summary of LAr Readout

LAr uses a three-gain structure to accommodate its large dynamic range. Each channel has a preamplifier and a 3-gain shaping amplifier before the SCA, as shown in Figure 1.

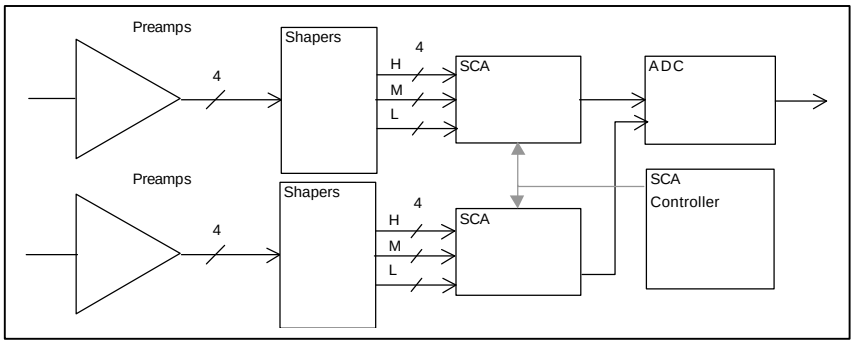

Figure 1. LAr tri-gain readout system

The SCAs each contain 16 "pipelines". Each pipeline is an array of 144 storage capacitors that can be connected to the read or write bus. The 12 shaped signals from 4 LAr channels are input to 12 of the pipelines and the remaining 4 pipelines are used as differential references (for subtraction of common mode noise.) All SCAs write to the same capacitor location in each pipeline. A new sample is written every 25 nsec. On readout, data from selected capacitors is multiplexed onto a common output bus. Only one sample at a time can be read out. The time required to read out a sample is limited by the settling time of the internal op-amp output buffer. A simplified block diagram of the SCA is shown in Figure 2.

Data can be simultaneously read and written to the SCA.

As shown in Figure 1, a pair of SCAs is read out by a dedicated 12 bit ADC. Each SCA pair has a dedicated readout controller chip. Write addresses are generated by a central controller.

Upon receipt of a Level 1 trigger, the readout cycle is started. The SCA controller first reads out the peak sample in the mid-gain range of all channels to determine the proper gain for each channel. Then 5 samples from the proper gain range of all channels are read out. Hence the readout time is 8 + 5 x 8 = 48 read clocks. With a readout clock of 5 MHz the read cycle can be completed in less than 10 μs, allowing an average trigger rate of 100 kHz. This 5-sample readout cycle is shown in Figure 3 below.

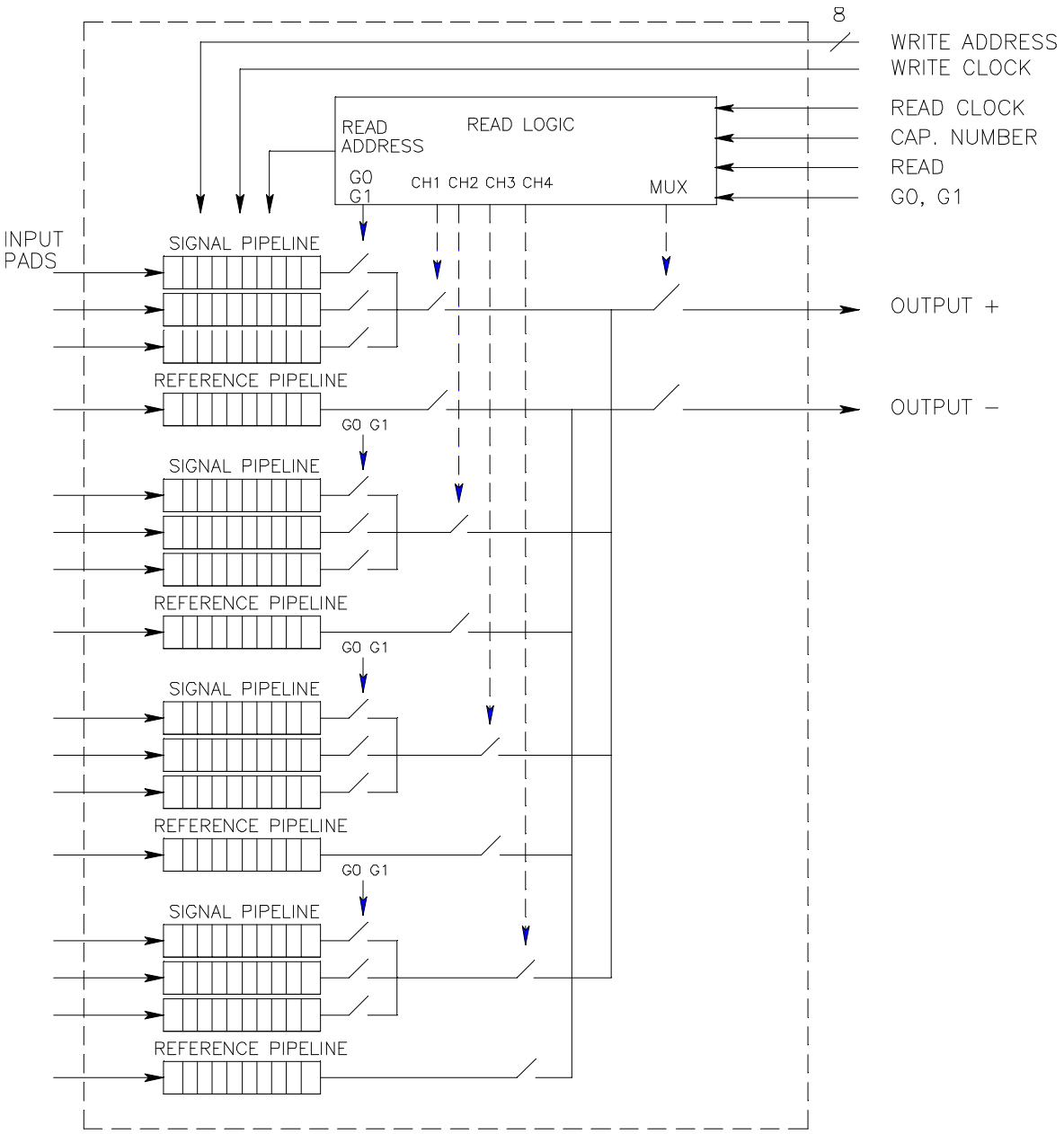

Figure 2. Simplified block diagram of the HAMAC SCA chip.

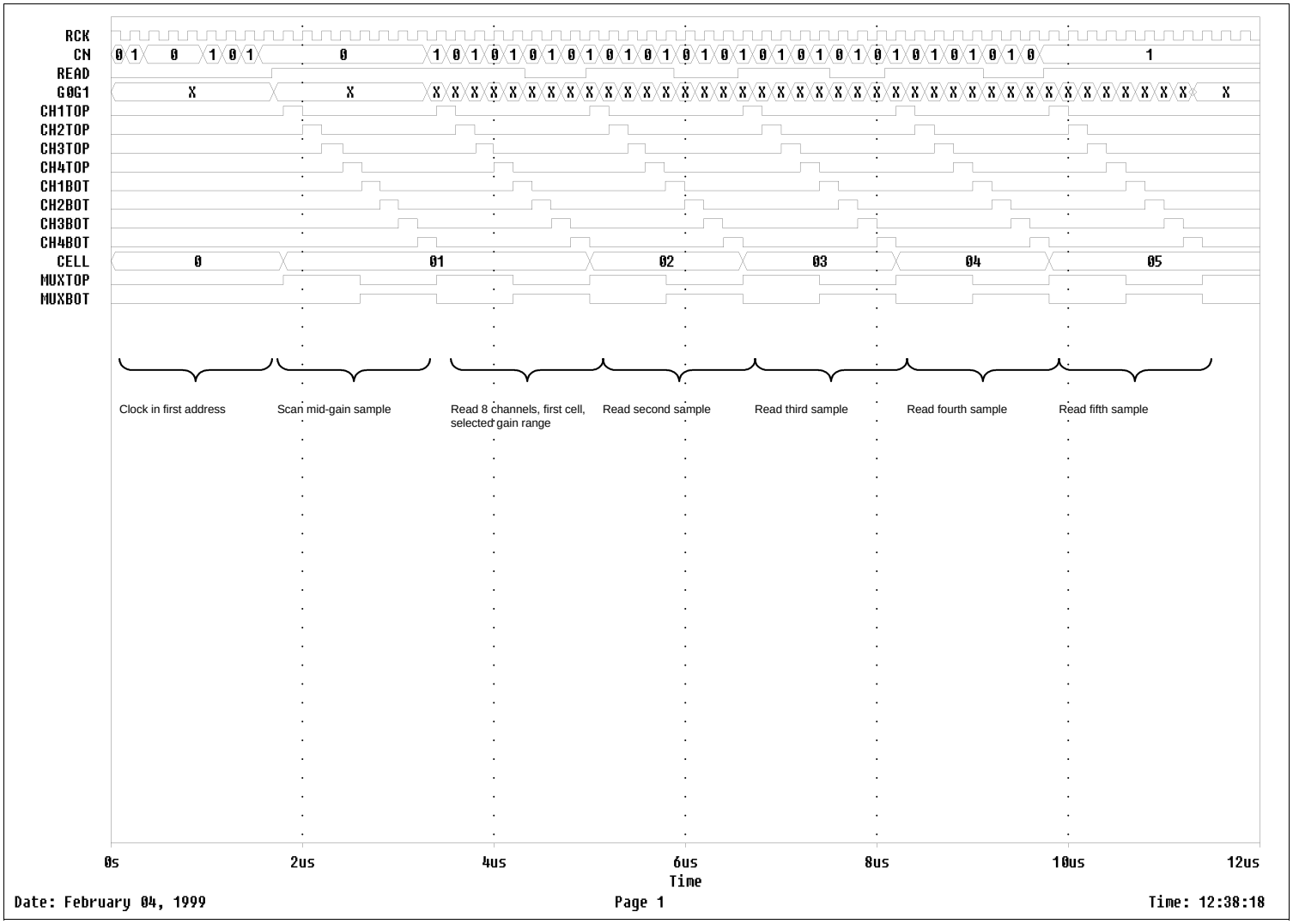

Figure 3. Simplified timing of the SCA readout cycle.

Readout electronics is implemented as a 128 channel Front End Board (FEB.) The crate-mounted FEB holds the input connectors, preamp hybrids, shapers, SCAs, SCA controller FPGAs, clock and power distribution, calibration, and off-board optical transmitters. The preamps, shapers, and SCAs are mounted on both sides of the FEB. The top and bottom SCA chips have mirror-image pinouts to minimize board area and allow easier signal bussing. A layout drawing of a non-radiation hardened prototype FEB is shown in Figure 4. The final version of the FEB is required to withstand radiation up to 100 krad and 5 $x10^{13}$ neutrons/cm^2.

The SCA is packaged in a 100-lead QFP measuring approximately 17.8 x 25.4 mm. A portion of the FEB showing the top-side SCAs is shown in Figure 5.

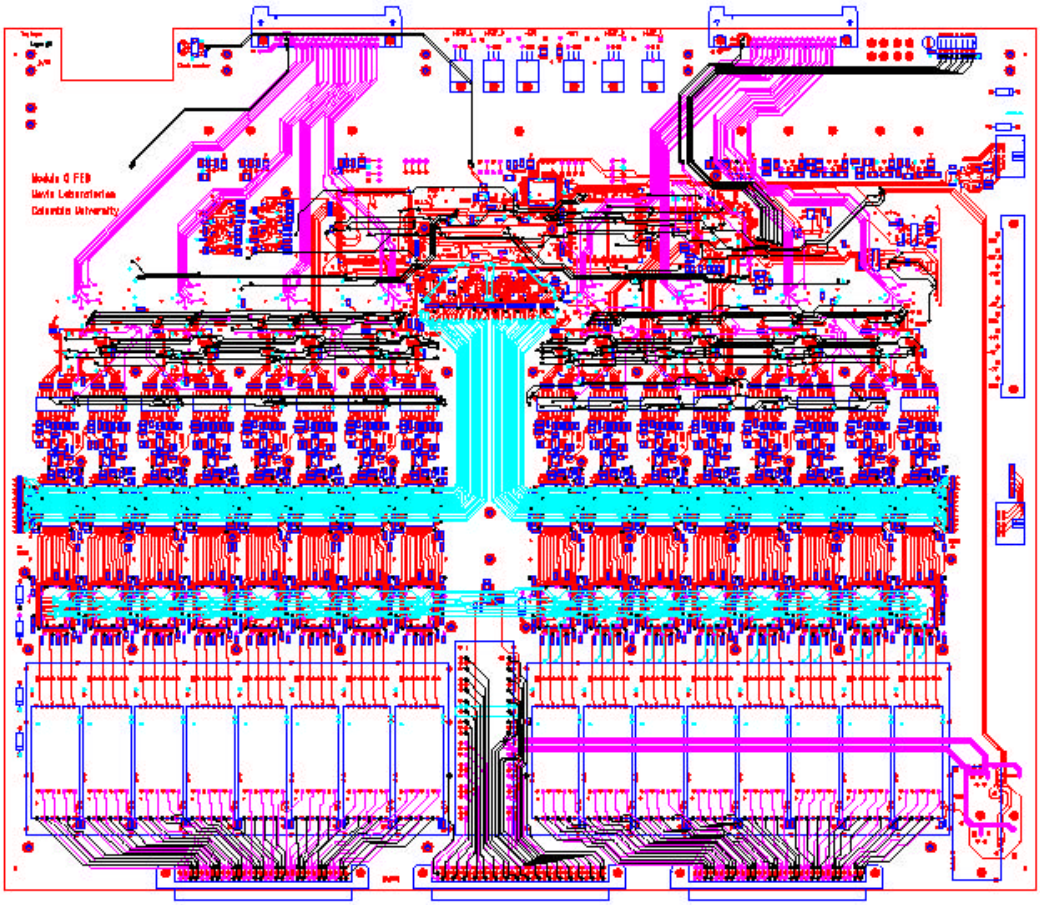

Figure 4. Layout of the LAr front-end board (FEB). Overall size: 49 x 41 cm.

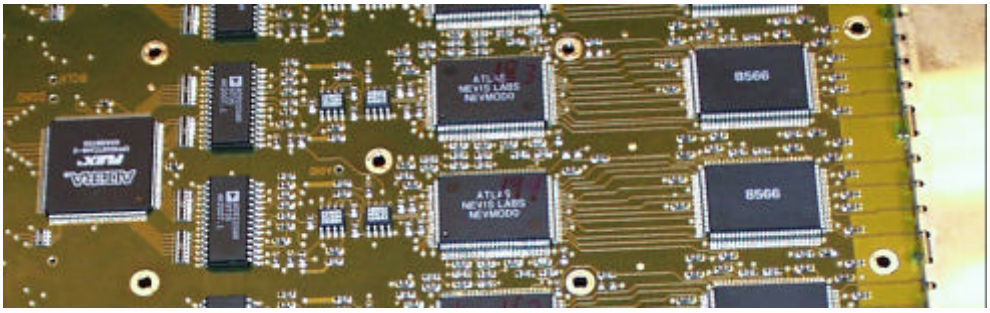

Figure 5. Photograph of a portion of FEB showing (right to left) shapers ("8566"), SCAs, ADCs, and SCA readout controller.

Proposal for CSC readout

Although it was designed for LAr's tri-gain readout configuration, the HAMAC SCA can also be used for single-gain systems such as the ATLAS CSC. In this case the 12 data pipelines are driven by 12 independent, single-gain shapers. During readout, "Gain Select" addresses G0, G1 must be used in conjunction with the built-in readout sequencer to control the order in which channels are read out.

If we use the HAMAC SCA as a memory for 12 single-gain channels, we effectively triple the multiplexing ratio into the ADCs. That is, each ADC would now serve 24 channels compared to 8 channels in the tri-gain LAr system. To achieve the same readout time, the Read Clock rate would need to increase. After accounting for the overhead in the first gain-selecting pass in the tri-gain system, the single-gain system would need to run with a Read Clock 2.5 times faster. At this speed, the settling of the SCA output buffer amplifier would become a serious concern.

In order to avoid the potential degradation caused by the high Read Clock rate, the LAr group was asked to modify the SCA output sequencing logic. The modified chip (HAMAC v.3) incorporates an optional "MUON" mode which changes the readout sequence from 1:8 to 1:4. Now 24 channels can be read out in 15 Read Clock cycles rather than 24, by allowing every SCA chip to drive its own ADC. Earlier versions of the chip required 2 SCAs to multiplex into one ADC (compare Fig. 1 and Fig. 6) This increased parallelism means that the Read Clock rate only has to increase by a factor of 1.56 to complete a 5-sample readout in 10 μs. In CALORIMETER mode five samples are read out in 48 Read Clock cycles; in MUON mode, the ADC serves 12 channels and 75 Read Clock rate cycles are needed to read out 5 samples.

In fact, we plan to run the CSCs with only 4 samples at high trigger rates, so the Read Clock rate increases by only 25% compared to the LAr FEB. This modest increase in clock rate is not expected to unduly degrade the accuracy of the readout.

The HAMAC v.3 design was submitted to the DMILL foundry in May 1999. Samples of chips from a valid fabrication lot were received at Brookhaven Laboratory in June, 2000.

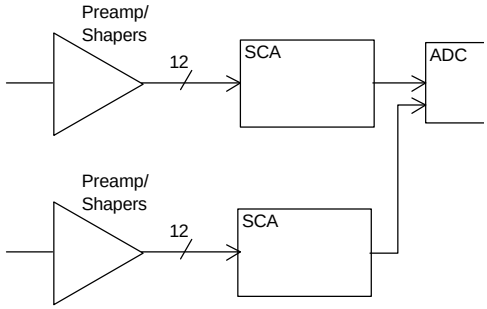

Figure 6. Proposed configuration of Nevis SCAs in the CSC system.

Other differences

Several other important differences between the CSC and LAr readout electronics will be briefly highlighted.

A. Signal levels and power supply.

Both LAr and CSC plan to DC-couple the shapers to the SCA. In the LAr system the shaper baseline is at 0V DC, while the CSC preamp/shaper has its baseline at 1.5V DC. The LAr scheme uses offset power

supplies of -1.7V and +3.3V on the SCA, allowing them to measure signals in the range of -0.9V to +2.5V. In the CSC however, the signal range is from 0V to +3.2V. We would need offset power supplies of -0.9V and +4.1V to record both lobes of the full-scale signal. To avoid the difficulty of providing these offset supplies, 0V and +5V rails will be used on the CSCs and the negative lobes of the largest pulses will be clipped. (During normal data taking no samples on the negative lobe are used.) The digital inputs to the SCA will be unaffected because the PECL drivers generating these signals will run off the same negative supply rail as the CSC in both the LAr and CSC systems.

B. Sampling rate and number of samples

The LAr system records samples every 25 ns and transmits 5 samples in response to every trigger. The CSC needs to restrict the output data bandwidth and therefore we plan to send only 4 samples per trigger. With 40 MHz sampling, the time window (time between first and last sample) is 75 ns. Since we can have up to 30 ns drift time uncertainty, this 75 ns window is too narrow -- it will not always contain the peak sample and two adjacent samples, all of which are needed for sparsification. Therefore, the CSC will sample at 20 MHz. It has been demonstrated by analysis of beam test data that position resolution and efficiency are no worse at 20 MHz sampling than at 40 MHz.

C. Location of the SCA controller

In each FEB in the LAr system, the SCA Write Addresses are generated by Controller chips (2 per FEB) and Read Addresses by Gain Selector chips (16 per FEB). Each of these is a high gate count digital IC clocked at 40 MHz, for which radiation-tolerant implementations are still being developed.

The CSC on-detector electronics has less space, less cooling, and more radiation than the LAr FEB. Therefore, SCA control functions will be located in the Sparsifier boards in the counting room and control signals will be transmitted to each ASM boards over optical fiber. The control link requires approximately the same bandwidth as the data links and the same G-link and optical transceiver will be used.

D. Data rate

The raw data rate coming off the LAr FEB at 100 kHz trigger rate is about 900 Mbit/s:

$$128 \text{ chan} \times 5 \text{ samples} \times (12 + 2 \text{ bits}) \times 10^5 \text{ s}^{-1} = 896 \text{ Mbit/s}$$

In the CSCs with 4 samples the corresponding raw data rate is very similar:

$$192 \text{ chan} \times 4 \text{ samples} \times 12 \text{ bits} \times 10^5 \text{ s}^{-1} = 922 \text{ Mbits/s}$$

E. Area and power consumption

	LAr-FEB	CSC-ASM	Units
Channels	128	192	
Gain ranges	3	1	
Total board area	2010	580	cm^2
Power dissipation	85	35	W